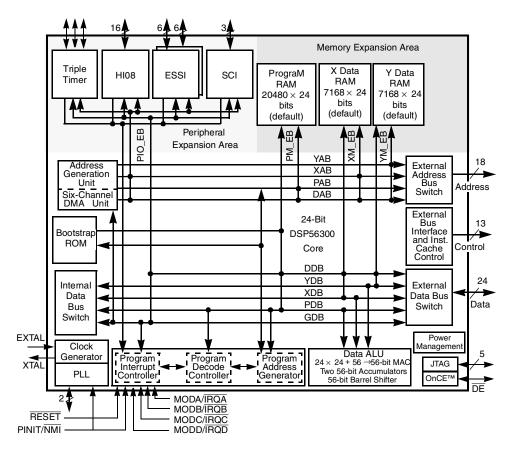
### Freescale Semiconductor Product Brief Advance Information

# **DSP56309**

### 24-Bit Digital Signal Processor



The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.

Figure 1. DSP56309 Block Diagram

The DSP56309 is a member of the DSP56300 core family of programmable CMOS DSPs. The DSP56300 core includes a barrel shifter, 24-bit addressing, an instruction cache, and direct memory access (DMA). The DSP56309 offers 100 million multiply-accumulates per second (MMACS) at 3.0–3.6 V using an internal 100 MHz clock. The large internal memory is ideal for wireless infrastructure and wireless local-loop applications. The DSP56300 core family offers a new level of performance in speed and power provided by its rich instruction set and low-power dissipation, thus enabling a new generation of wireless, multimedia, and telecommunications products.

Note: This document contains information on a new product. Specifications and information herein are subject to change without notice.



© Freescale Semiconductor, Inc., 1996, 2005. All rights reserved.

## Features

 Table 1 lists the features of the DSP56309 device.

Feature	Description						
High-Performance DSP56300 Core	<ul> <li>100 million multiply-accumulates per second (MMACS) with a 100 MHz clock at 3.3 V nominal</li> <li>Data arithmetic logic unit (Data ALU) with fully pipelined 24 × 24-bit parallel multiplier-accumulator (MAC), 56-bit parallel barrel shifter (fast shift and normalization; bit stream generation and parsing), conditional ALU instructions, and 24-bit or 16-bit arithmetic support under software control</li> <li>Program control unit (PCU) with position-independent code (PIC) support, addressing modes optimized for DSP applications (including immediate offsets), internal instruction cache controller, internal memory-expandable hardware stack, nested hardware DO loops, and fast auto-return interrupts</li> <li>Direct memory access (DMA) with six DMA channels supporting internal and external accesses; one-, two-and three-dimensional transfers (including circular buffering); end-of-block-transfer interrupts; and triggering from interrupt lines and all peripherals</li> <li>Phase-lock loop (PLL) allows change of low-power divide factor (DF) without loss of lock and output clock with skew elimination</li> <li>Hardware debugging support including on-chip emulation (OnCE) module, Joint Test Action Group (JTAG) test access port (TAP)</li> </ul>						
Internal Peripherals	<ul> <li>Enhanced 8-bit parallel host interface (HI08) supports a variety of buses (for example, ISA) and provides glueless connection to a number of industry-standard microcomputers, microprocessors, and DSPs</li> <li>Two enhanced synchronous serial interfaces (ESSI), each with one receiver and three transmitters (allows six-channel home theater)</li> <li>Serial communications interface (SCI) with baud rate generator</li> <li>Triple timer module</li> <li>Up to thirty-four programmable general-purpose input/output (GPIO) pins, depending on which peripherals are enabled</li> </ul>						
Internal Memories	<ul> <li>192 × 24-bit boo</li> <li>8 K × 24-bit RAI</li> <li>Program RAM, i</li> <li>Program RAM</li> <li>Size</li> <li>20480 × 24 bits</li> <li>19456 × 24 bits</li> <li>24576 × 24 bits</li> <li>23552 × 24 bits</li> </ul>	M total	X data RAM, and $\stackrel{?}{}$ X Data RAM Size 7168 $\times$ 24 bits 7168 $\times$ 24 bits 5120 $\times$ 24 bits 5120 $\times$ 24 bits	Y data RAM sizes a Y Data RAM Size 7168 $\times$ 24 bits 7168 $\times$ 24 bits 5120 $\times$ 24 bits 5120 $\times$ 24 bits	are programmable Instruction Cache disabled enabled disabled enabled	e: Switch Mode disabled disabled enabled enabled	
External Memory Expansion	<ul> <li>Data memory expansion to two 256 K × 24-bit word memory spaces using the standard external address lines</li> <li>Program memory expansion to one 256 K × 24-bit words memory space using the standard external address lines</li> <li>External memory expansion port</li> <li>Chip select logic for glueless interface to static random access memory (SRAMs)</li> <li>Internal DRAM Controller for glueless interface to dynamic random access memory (DRAMs)</li> </ul>						
Power Dissipation	<ul> <li>Very low-power CMOS design</li> <li>Wait and Stop low-power standby modes</li> <li>Fully static design specified to operate down to 0 Hz (dc)</li> <li>Optimized power management circuitry (instruction-dependent, peripheral-dependent, and mode-dependent)</li> </ul>						
Packaging	<ul> <li>144-pin TQFP package in lead-free or lead-bearing versions</li> <li>196-pin molded array plastic-ball grid array (MAP-BGA) package in lead-free or lead-bearing versions</li> </ul>						

Table 1.	DSP56309	Features
----------	----------	----------

### **Target Applications**

The DSP56309 is intended for applications benefiting from a large amount of internal memory, such as wireless infrastructure applications.

### **Product Documentation**

The documents listed in **Table 2** are required for a complete description of the DSP56309 device and are necessary to design properly with the part. Documentation is available from a local Freescale distributor, a Freescale semiconductor sales office, or a Freescale Semiconductor Literature Distribution Center. For documentation updates, visit the Freescale DSP website. See the contact information on the back cover of this document.

Name	Description	Order Number	
DSP56309 Technical Data	Description, features list, and specifications of the DSP56309	DSP56309	
DSP56309 User's Manual	Detailed functional description of the DSP56309 memory configuration, operation, and register programming	DSP56309UM	
DSP56300 Family Manual	Detailed description of the DSP56300 family processor core and instruction set	DSP56300FM	
Application Notes	Documents describing specific applications or optimized device operation including code examples	See the DSP56309 product website	

### Table 2. DSP56309 Documentation

#### How to Reach Us:

Home Page: www.freescale.com

E-mail: support@freescale.com

#### USA/Europe or Locations not listed:

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@freescale.com

#### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GMBH **Technical Information Center** Schatzbogen 7 81829 München, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

#### Japan:

Freescale Semiconductor Japan Ltd. Headquarters ARCO Tower 15F 1-8-1, Shimo-Meguro, Meguro-ku, Tokyo 153-0064, Japan 0120 191014 or +81 3 5437 9125 support.japan@freescale.com

#### Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd. **Technical Information Center** 2 Dai King Street Tai Po Industrial Estate Tai Po, N.T. Hong Kong +800 2666 8080 support.asia@freescale.com

For Literature Requests Only: Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217 1-800-441-2447 or 303-675-2140 Fax: 303-675-2150 LDCForFreescaleSemiconductor@hibbertgroup.com

DSP56309PB Rev. 1 2/2005

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 1996, 2005.

